Numerical evaluations of a new 3D stacking structure for power supply on chip

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Abstract

- We propose the new 3D stacking structure for power supply on chip, which enable thermal insulation and heat exhausting.
- We also evaluate the proposed structure and compare proposed structure and the conventional one through numerical simulations.

Introduction

Power SoC

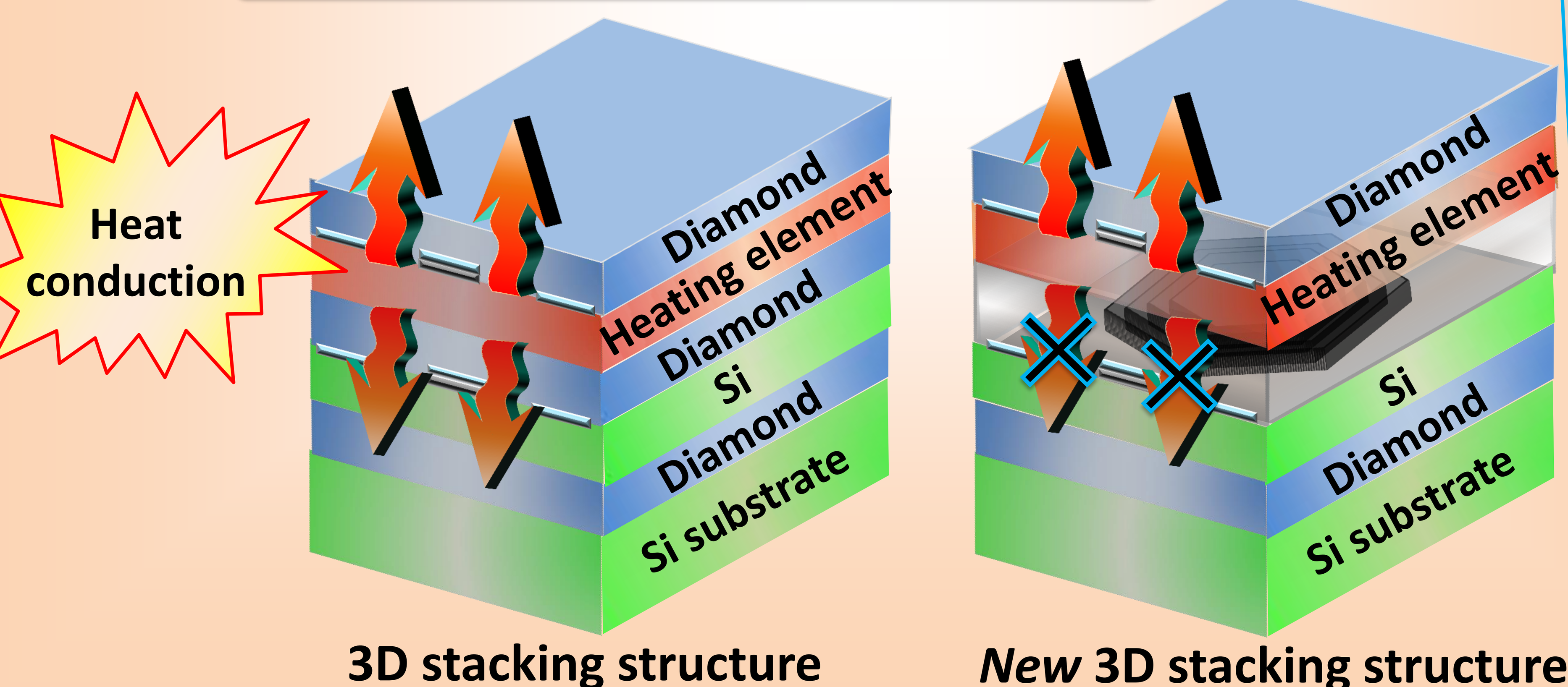
Merit
- Ultimate miniaturization
- Mass production

Challenges…
- Self heating
- High frequency switching

3D stacking structure

Heat insulation & Exhausting heat

Thick SiO_2 with glass interposer



3D stacking structure — *New* 3D stacking structure

Simulation condition

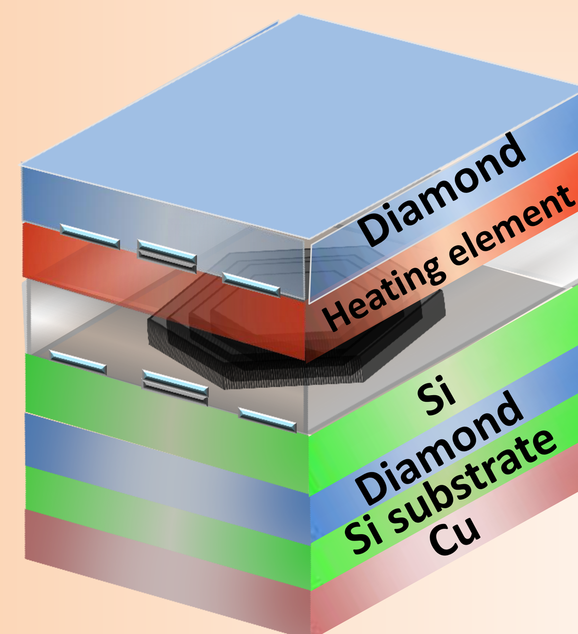
•***Thermal analysis***

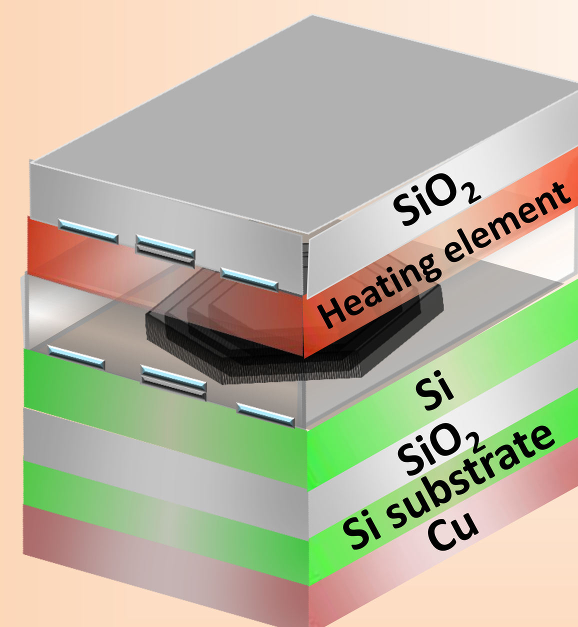
$$\rho c \frac{\partial T}{\partial t} = \frac{\partial}{\partial x}\left(\lambda \frac{\partial T}{\partial x}\right) + \frac{\partial}{\partial y}\left(\lambda \frac{\partial T}{\partial y}\right) + Q_v$$

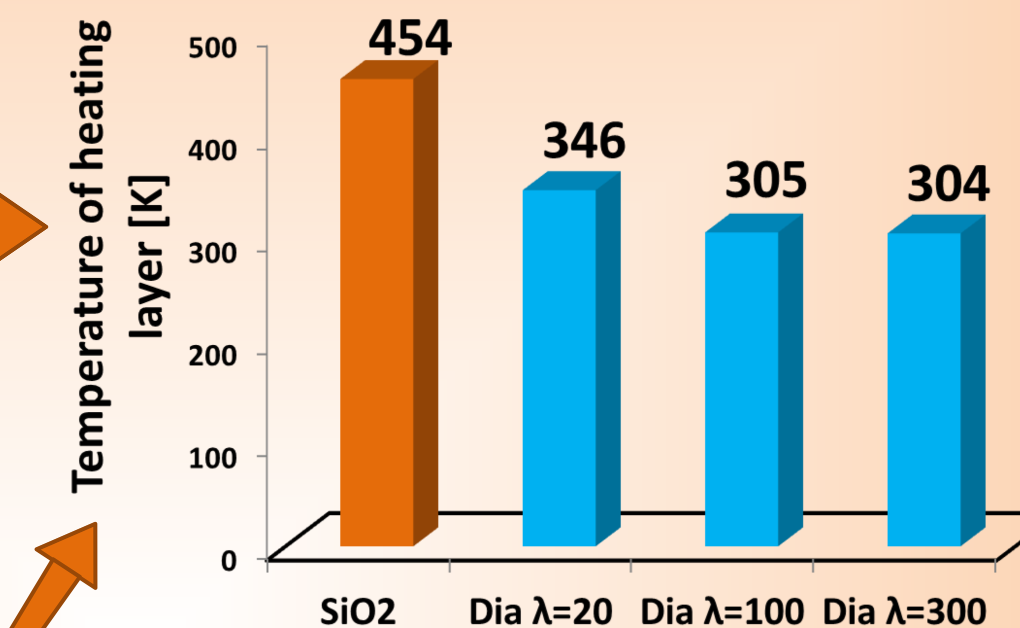
ρ: Density, c: specific heat capacity T: temperature, t: time, λ: thermal conductivity, Q_v: heat generation

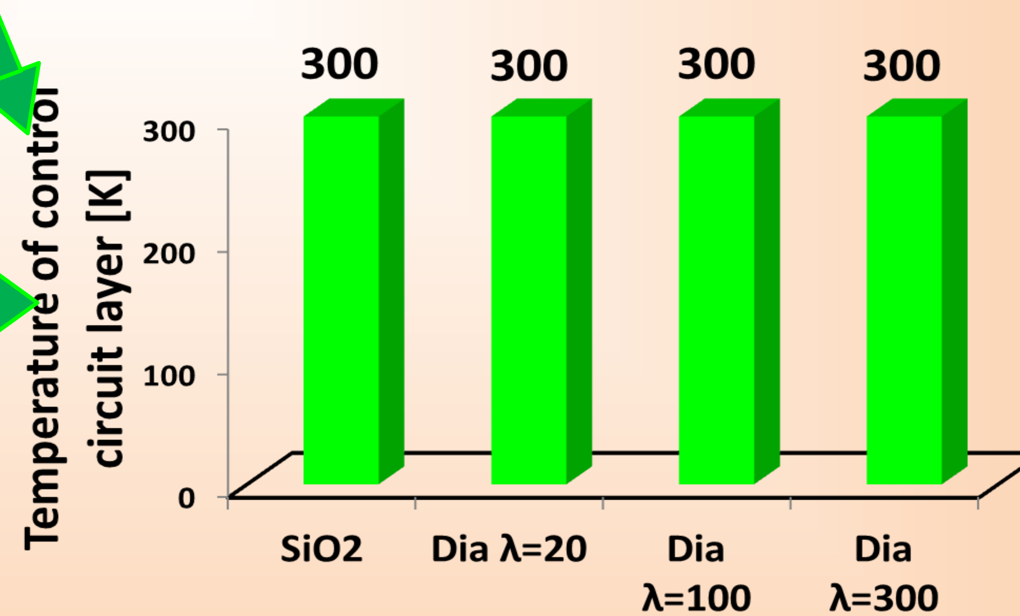
•Giving 1W for heating layer

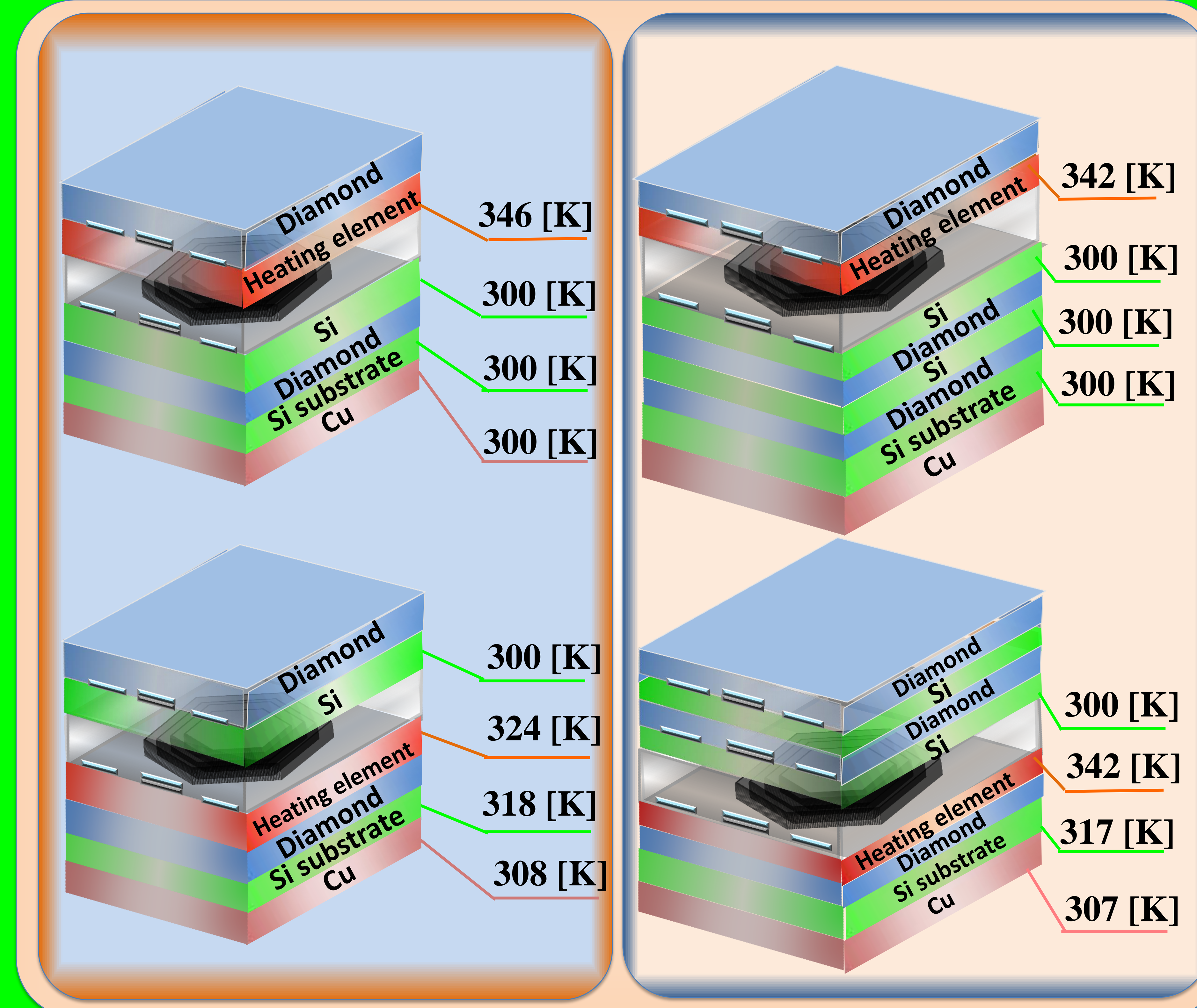
Simulation & Results











Conclusions & Future work

- ***Heat insulation*** and ***Exhausting heat*** are important factor for 3D stacking structure
- Thin diamond film can realize exhaust heat and thick insulator can realize heat insulation
- Fabrication of 3D stacking structure